



# Table of Contents

<b>Preface .....</b>	<b>xiii</b>
<b>Chapter 1: Introduction to VLSI Design .....</b>	<b>1</b>
Traditional Approach to Hardware Design .....	2
New Paradigms in Hardware Design .....	3
VLSI Technology: Fundamentals and Applications .....	4
Advantages of VLSI Technology .....	4
Challenges in VLSI Technology .....	4
Evolution of the Integration Levels .....	5
VLSI Design Process.....	6
VLSI Design Methodology.....	7
How to Specify a System?.....	7
How to Convert Specifications into a Chip? .....	8
Electronic Design Automation.....	9
ASIC .....	9
ASIC Design Flow .....	10
Field Programmable Gate Array (FPGA).....	10
FPGA Design Flow .....	11
System on Chip Designs.....	13
Summary.....	14
Review Questions.....	14
<b>Chapter 2: VLSI Design Technologies.....</b>	<b>15</b>
Combinatorial Design Technique .....	16
Boolean Equation.....	19
Schematic .....	19
Canonical Form.....	21
Standard Form .....	22
Factored Form.....	22
Don't Care Combinations.....	22

**Table of Contents**

---

Sequential Design Technique.....	26
Synchronous Sequential Circuits.....	27
Asynchronous Sequential Circuits.....	31
State Machine Logic Design Technique.....	31
Design Issues .....	34
Fan-Out.....	34
Meta-Stability.....	34
Timing.....	35
Summary.....	36
Review Questions.....	36
Exercises.....	36
<b>Chapter 3: CMOS VLSI Design.....</b>	<b>37</b>
MOS Technology and Fabrication Process.....	38
Fabrication Process.....	38
pMOS.....	41
nMOS.....	42
CMOS.....	44
The p-well Process.....	44
The n-well Process.....	45
The twin-tub Process.....	45
BiCMOS.....	46
Comparison of Different Processes.....	46
Power Dissipation.....	46
Propagation Delay.....	47
Summary.....	47
Review Questions.....	48
Exercises.....	48
<b>Chapter 4: Building Blocks of a VLSI Circuit.....</b>	<b>49</b>
Computer Architecture.....	50
MUX.....	50
Decoder.....	52
Priority Encoder.....	53
Magnitude Comparator.....	54
Bit-Adder.....	55
Memory Architectures.....	57
Shifter.....	57
ROM.....	58
RAM.....	59

Communication Interfaces .....	59
Parallel Data Transmission .....	60
Parallel Communication Interface .....	61
Mixed Signal Interfaces .....	61
Summary .....	61
Review Questions .....	62
Exercises .....	62
<b>Chapter 5: VLSI Design Issues .....</b>	<b>63</b>
Design Process .....	64
Design for Testability .....	64
What is testing? .....	65
Fault Coverage .....	66
The Single Stuck-At Fault Model .....	66
Technology Options .....	67
Full-Custom Design .....	67
Semi-Custom Design .....	68
Cell-Based Designs .....	68
Array-Based Designs .....	69
Power Calculations .....	70
Package Selection .....	70
Clock Mechanisms .....	71
Mixed Signal Design .....	73
Summary .....	74
Review Questions .....	74
<b>Chapter 6: EDA Tools: An Overview .....</b>	<b>75</b>
EDA .....	76
Taxonomy of Tools .....	76
Altera's Quartus II Software .....	79
Microwind Tools .....	79
Xilinx Tools .....	79
Architecture Design .....	79
Top-Down Design .....	80
Bottom-Up Design .....	80
Design Entry .....	81
Schematic Editor .....	81
VHDL Editor/Verilog Editor .....	82
Block Editor .....	82

**Table of Contents**

---

Synthesis Tools: XST, Synplify, and Leonardo Spectrum.....	83
Creating a new Project using the Xilinx Project Navigator .....	83
Functional Verification.....	97
Black Box Verification .....	98
White Box Verification .....	98
Timing Verification.....	99
On-Chip Debugging.....	99
Summary.....	100
Review Questions.....	100
Exercises.....	100
<b>Chapter 7: HDL Simulation and Synthesis.....</b>	<b>101</b>
Overview of VHDL .....	102
VHDL Code Structure.....	103
Syntax and Semantics of VHDL.....	104
NOT Gate.....	106
OR Gate.....	108
AND Gate .....	111
NOR Gate.....	113
NAND Gate .....	115
XOR Gate .....	117
XNOR Gate .....	119
D Flip-Flop.....	121
VHDL Implementation .....	121
Decade Counter .....	124
Overview of Verilog.....	127
Verilog Code Structure.....	128
Syntax and Semantics of Verilog .....	129
Data Types .....	130
Data Objects .....	130
NOT Gate.....	130
OR Gate.....	131
AND Gate .....	132
NOR Gate.....	133
NAND Gate .....	133
XOR Gate .....	134
XNOR Gate .....	134
D Flip-Flop.....	135
Counter .....	136

Simulation.....	136
Synthesis .....	137
Behavioral Modeling.....	140
Timing Analysis.....	141
RTL Simulation.....	141
VITAL Simulation .....	141
Summary.....	142
Review Questions.....	142
Exercises.....	142
<b>Chapter 8: IC Design .....</b>	<b>143</b>
PLAs.....	144
PLDs.....	146
FPGA.....	148
Antifuse FPGA.....	149
Flash FPGA .....	150
SRAM FPGA.....	150
ASIC .....	151
Selection of an Appropriate Integrated Circuit.....	151
Summary.....	151
Review Questions.....	152
Exercises.....	152
<b>Chapter 9: FPGA Design Process.....</b>	<b>153</b>
Architectures of Popular FPGAs.....	154
Basic FPGA Architecture.....	154
Choosing an FPGA .....	156
IP Cores.....	156
FPGA Configuration.....	157
Configuration Modes .....	158
FPGA Design Process .....	159
FPGA Design Flow .....	159
Designing FPGA-Based PCBs.....	161
FPGA Families of Different Vendors.....	163
Illustration: FPGA Families of Xilinx.....	163
FPGA Design Examples .....	164
Stack Implementation using VHDL.....	164
Device Utilization Summary.....	169
Queue Implementation using VHDL .....	170
Shift Register implementation using VHDL .....	175

**Table of Contents**

---

Summary.....	179
Review Questions.....	179
Exercises.....	180
<b>Chapter 10: VHDL Implementation Examples .....</b>	<b>181</b>
Adder .....	182
Multiplier .....	186
Multiplexer .....	192
16 X 1 Multiplexer.....	195
Summary.....	198
Review Questions.....	198
<b>Chapter 11: Case Study: Xilinx Development Board .....</b>	<b>199</b>
Xilinx ISE 10.1 .....	200
Design Entry in HDL/Schematic.....	200
Simulation and Synthesis (Design Verification) .....	201
Design Implementation.....	201
Development Board Architecture.....	201
Interfacing with Peripherals.....	202
Summary.....	208
Review Questions.....	208
Exercises.....	208
<b>Chapter 12: Case Study: Implementation of a Communication System.....</b>	<b>209</b>
Xtreme DSP Board Overview.....	210
The Xtreme DSP Kit for Virtex-4.....	210
Design Details.....	212
Implementation Details.....	212
Creating a New Project using the Xilinx Project Navigator .....	213
Generation of 1 KHz Sine Wave (Tone) Component .....	217
Simulation.....	225
Simulation in ModelSim.....	226
AM Modulator Implementation .....	231
Simulation Results of AM Modulation.....	238
AM Demodulation.....	238
Envelope Detector .....	238
AM Demodulation Simulation Results .....	246
Device Utilization.....	247
Testing Environment.....	247
Testing the Code on FPGA Development Board .....	247
Challenges in Signal Processing using FPGA .....	261
Summary.....	261
Review Questions.....	261
Exercises.....	262

---

<b>Chapter 13: Case Study: System-On-Chip Development .....</b>	<b>263</b>
System-On-Chip Requirements .....	263
Design .....	265
Hard Core/Hard IP .....	266
Soft Core/Soft IP .....	266
Firm Core/Firm IP .....	266
Implementation .....	266
Selection of Platform based on Application .....	267
Summary .....	268
Review Questions .....	268
Exercises .....	268
<b>Chapter 14: Future Trends .....</b>	<b>269</b>
Ubiquitous Computing and Pervasive Computing Technologies .....	270
VLSI Design Trends .....	271
Summary .....	273
<b>Appendix A: VHDL and Verilog Examples .....</b>	<b>275</b>
<b>Appendix B: Internet Resources .....</b>	<b>327</b>
<b>Appendix C: Acronyms and Abbreviations .....</b>	<b>329</b>
<b>Glossary .....</b>	<b>335</b>
<b>Index .....</b>	<b>341</b>